REMARKS

In the Official Action mailed on **22 March 2006**, the Examiner reviewed claims 1, 3-9, 11-17, and 19-27. Claims 1, 3, 4, 6-9, 11, 12, 14-17, 19, 20, and 22-27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Li et al (USPN 6,208,183, hereinafter "Li") in view of any one of Self et al. (USPN 6,112,308 hereinafter "Self '308"), (USPN 6,009,532 hereinafter "Self '532") in view of Bar-Niv (USPN 5,631,591 hereinafter "Bar-Niv"), in view of Oman et al. (USPN 4,635,186 hereinafter "Oman"), in view of Eggebrecht et al. (USPN 4,495,594 hereinafter "Eggebrecht), in view of Lenk (USPN 6,538,516 hereinafter "Lenk"), in view of Chesavage (USPN 6,239,626 hereinafter "Chesavage '626"), in view of Locker et al. (USPN 6,577,174 hereinafter "Locker"), in view of Doblar et al. (USPN 6,516,422 hereinafter "Doblar"), in view of Smith et al. (USPN 6,925,135 hereinafter "Smith"), in view of Yabuki et al. (USPN 5,332,978 hereinafter "Yabuki"). and further in view of Chesavage (USPN 6,925,135 hereinafter "Chesavage '350"). Claims 5, 13, and 21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Li et al. any one of Self '308, Self '532 in view of Bar-Niv, Oman, Eggebrecht, and further in view of any one Lenk, Chesavage '626, Locker et al., Doblar et al., Smith et al., Yabuki et al., Chesavage '350, and further in view of Coleman et al (USPN 4,151,473, hereinafter "Coleman").

Rejections under 35 U.S.C. §103(a)

Independent claims 1, 9, and 17 were rejected as being unpatentable over Li in view of any one of Self '308, Self '532, Bar-Niv, Oman, and Eggebrecht and further in view of any one of Lenk, Chesavage '626, Locker, Doblar, Smith, Yabuki, Chesavage '350, and Coleman.

Applicant respectfully points out that the **cited prior art requires that the phase-lock loop (PLL) circuits be able to detect each others' frequencies**. For instance, Coleman (col. 3, lines 25-30), Self '308 (col. 9, lines 15-25), and Bar-

Niv (col. 4, 47-64) depend on being able to detect the phase difference between the frequencies of two circuits, or on using a separate reference clock (Li, col. 7, lines 23-42, Self '308, col. 8, lines 1-10, and Bar-Niv, col. 2, lines 58-63) with a phase or frequency that all circuits can detect.

Applicant notes that a large disparity between the initial frequency or speed of the local chip and the neighboring chip can result in the slower chip mistaking the frequency signal of the faster chip as a DC signal. This condition is handled by the present invention (page 9, line 21 to page 10, line 2 of the instant application). Note that while the slower chip may not detect the speed of the faster chip, and may as a result slow down its operation or otherwise incorrectly change its operating speed, the faster chip **will** be able to detect the frequency signal of the slower chip. Hence in one embodiment of the present invention, the faster chip is configured to detect the speed disparity and to slow down until, eventually, the control loop of the slower chip can correctly recognize the faster chip's frequency signal, and respond correctly. At that point, the local chip and the neighboring chip can negotiate a maximum common frequency.

Applicant points out that nothing in Li in view of any one of Self '308, Self '532, Bar-Niv, Oman, and Eggebrecht and further in view of any one of Lenk, Chesavage '626, Locker, Doblar, Smith, Yabuki, Chesavage '350, and Coleman teaches a method for generating a maximum common frequency that enables chips to communicate with each other without a reference clock when there exists a sufficient disparity in frequencies that one chip cannot detect the frequency of the other.

Accordingly, Applicant has amended independent claims 1, 9, and 17 to clarify that the present invention can handle a disparity between the initial speeds of the local chip and the neighboring chip that results in the slower chip mistaking a frequency signal of the faster chip as a DC signal. These amendments specify that the faster chip detects the frequency signal of the slower chip, and slows

down until the control loop of the slower chip can correctly recognize the faster chip's frequency.

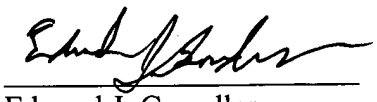
These amendments find support from page 9, line 21 to page 10, line 2 of the instant application.

Hence, Applicant respectfully submits that independent claims 1, 11, 14, and 20, as presently amended are in condition for allowance. Applicant also submits that claims 3-8 and 25, which depend upon claim 1, claims 11-16 and 26, which depend upon claim 9, and claims 19-24 and 27, which depend upon claim 17, are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

By 

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